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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/739,956	12/19/2000	David Neil Pether	00-332 1496.00075	6411

24319 7590 03/10/2004

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EXAMINER	
ARNOLD, ADAM	
ART UNIT	**PAPER NUMBER**
2671	11

DATE MAILED: 03/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/739,956	PETHER ET AL.	
	Examiner	Art Unit	
	Adam Arnold	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-11 and 13-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11 and 13-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The examiner acknowledges the receipt and entry of the applicant's amendment.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 20 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy, U.S. Patent No. 6,348,919 in view of Chamberlin, U.S. Patent No. 4,255,785. Referring to claim 1, Murphy discloses an apparatus for generating a region of graphics on a display (col. 1, line 13), the apparatus comprising: a bus serving a range of addresses (Figure 5C); a plurality of registers (col. 13, line 28) within an address range (col. 14, line 21) configured to store an x coordinate and a y coordinate of a pixel to be drawn (col. 14, lines 8-9); a calculation circuit configured to calculate an address for storage of data corresponding to the pixel in dependence on the x and y coordinates (col. 27, lines 1-14); and a control circuit configured to control writing of said data in memory at said address (see Figure 5D and col. 62, line 7) by driving the address onto the bus (as pointed out below, a bus transfers data throughout the computer; as such, data must be driven onto the bus to be usable). Murphy does not explicitly disclose a bus having a first address range and a second address range or a memory directly connected to the bus and responsive within the second address range. Chamberlin discloses multiple address ranges and a memory directly coupled to the bus and to the address

registers (col. 2, lines 44-47 and Figure 1, reference nos. 83 and 79). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a bus with a first address range and a second address range and to couple the memory directly to a bus. One of ordinary skill in the art would have been motivated to do this because buses serve as conduits for data exchange within a computer system. Moreover, a memory address is inherently broken up into different ranges. That is, each individual address or a group of addresses serve as a separate range from another address or group of addresses. Finally, by coupling the bus directly to memory, processing speed is increased (see col. 1, lines 60-63 of Chamberlin).

Referring to claim 3, Murphy further discloses a clipping circuit that serves to determine which coordinates fall outside of a particular threshold (col. 13, lines 39-41).

Referring to claim 4, Murphy does not explicitly disclose inhibiting writing of data to the address in response to the clipping circuit. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to inhibit writing of data to the address in response to the clipping circuit. One of ordinary skill in the art would have been motivated to do this because the purpose of a clipping circuit is to determine when pixel values are outside of a range, usually the viewing area. As such the values are extraneous and it is inherent that no further processing will be carried out on them.

Referring to claim 5, the remarks presented above with respect to claim 4 apply equally to this claim.

Referring to claim 6, the remarks presented above with respect to claim 4 apply equally to this claim.

Referring to claim 7, Murphy teaches a 1st register mapped to a 1st and 2nd location in memory and a 2nd register mapped to a 3rd and 4th location in memory (col. 13, lines 13-18 and 26-28, where each register is 32 bits, or 4 bytes, and each byte is a different location).

Referring to claim 20, Murphy in view of Chamberlin discloses a system for generating a region of graphics on a display as described fully in claim 1 above. The remarks directed to claim 1 above, apply equally to claim 20. The apparatus of Murphy performing the steps is recited in the claim.

Referring to claim 21, the remarks presented above with respect to claim 4 apply equally to this claim.

Referring to claim 22, the remarks presented above with respect to claim 7 apply equally to this claim.

Referring to claim 30, the remarks presented above with respect to claim 1 apply equally to this claim.

3. Claims 8-10 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy in view of Chamberlin, further in view of Chiu, U.S. Patent No. 5,796,391. Referring to claim 8, Murphy in view of Chamberlin discloses the graphics apparatus of claim 7. See 103 rejection above. Murphy does not teach an "address decoder" for monitoring the memory locations. Murphy does disclose monitoring the register's mapped addresses and subsequently writing the value and address tag to a FIFO buffer. Chiu teaches an address decoder attached to a control unit. See col. 3, line 45 and Figure 2, nos. 122 and 206. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have an address decoder for monitoring memory locations. One of ordinary skill in the art would have been

motivated to do this because, as pointed by the applicant, the sole purpose of the address decoder is to "monitor each of the four address locations N to N+3 to see which is written to and apply an address location signal to the write control unit 36" (page 8, lines 3-5 of Applicant's Amendment). Although Murphy doesn't use the Chiu terminology, the functionality is the same as the applicant's.

Referring to claim 9, the remarks presented above with respect to claims 1 and 8 apply equally to this claim.

Referring to claim 10, the remarks presented above with respect to claims 1 and 8 apply equally to this claim.

Referring to claim 23, the remarks presented above with respect to claims 8 and 22 apply equally to this claim.

Referring to claim 24, the remarks presented above with respect to claims 8 and 22 apply equally to this claim.

4. Claims 11, 13, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy in view of Chamberlin, further in view of Prouty, U.S. Patent No. 5,986,658. Murphy does not teach a style table for storing data corresponding to a predetermined style for the pixel, or a style counter for indexing the data in the style table. Prouty teaches a line style array for storing line style pattern features and a line style feature pixel counter. See Figure 2, elements 211 and 217. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a style table for storing data corresponding to a predetermined style for the pixel and a style counter for indexing the data in the style table. One of ordinary skill in the art would have been motivated to do this to provide for drawing complex line styles

in real time. See Prouty, col. 1, lines 4-9. Further, both references are directed to the generation and use of raster computer graphics (see col. 9, lines 67 of Murphy and lines 1-2 of the Prouty abstract). Thus, Prouty simply provides details of the generation of a specific type of graphic, the type being more generally described and used by Murphy.

Referring to claim 13, Murphy in view of Chamberlin does not teach a style table configured to store a non-repeating bit pattern up to a predetermined length. Prouty teaches an array large enough to handle line style pattern features. See Prouty, col. 7, line 29. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a style table configured to store a non-repeating bit pattern up to a predetermined length. One of ordinary skill in the art would have been motivated to do this to provide for different size bit patterns.

Referring to claim 14, the remarks presented above with respect to claims 8 and 11 apply equally to this claim.

Referring to claim 25, the remarks presented above with respect to claims 11 and 20 apply equally to this claim.

Referring to claim 26, Murphy in view of Chamberlin does not disclose selecting a color for the pixel to be drawn dependent on the style data signal. Prouty discloses that in a preferred embodiment of their invention, the style array records color information for the line. See col. 5, line 19. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a style table record color information for the pixel. One of ordinary skill in the art would have been motivated to do this to record accurate information regarding the graphics display as well as the reasons above.

5. Claim 15-19 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy in view of Chamberlin, further in view of Ozcelik, Patent Publication No. 2002/0149626. Referring to claim 15, Murphy does not teach outputting a word address corresponding to the address location in memory and a bit address representing a position of the pixel data within a word. Ozcelik teaches outputting a word address corresponding to the address location in memory and a bit address representing a position of the pixel data within a word. See paragraph 47. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to output a word address corresponding to the address location in memory and a bit address representing a position of the pixel data within a word. One of ordinary skill in the art would have been motivated to do this to increase flexibility in defining displays. See Ozcelik, paragraph 8. Further, Ozcelik provides the details of addressing memory for storage/retrieval of data such as done in Murphy.

Referring to claim 16, Murphy in view of Chamberlin, further in view of Ozcelik discloses the graphics apparatus described in claim 15. See 103 rejection above. Murphy further discloses a second register for storing pixel data (col. 16, lines 15-16) and a multiplexer (or logic unit, i.e., a device for performing digital logical analysis) for writing data to memory (see Figure 2B).

Referring to claim 17, Murphy in view of Chamberlin, further in view of Ozcelik discloses the graphics apparatus described in claim 16. See 103 rejection above. Murphy does not explicitly disclose that the multiplexer combines data for two or more pixels. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a multiplexer that combines data for two or more pixels. One of ordinary skill in the art would

have been motivated to do this because the purpose of a multiplexer is to combine signals for transmission over a medium.

Referring to claim 18, Murphy in view of Chamberlin, further in view of Ozcelik discloses the graphics apparatus described in claim 17. See 103 rejection above. Murphy discloses a comparator for comparing depth and color values (col. 75, line 57). Murphy does not disclose comparing addresses of pixels to be drawn. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to compare addresses of pixels. One of ordinary skill in the art would have been motivated to do this because comparison operations are frequently used in graphics processing to preserve physical memory.

Referring to claim 19, the remarks directed to claims 1 and 18, above, apply equally to this claim.

Referring to claim 27, the remarks directed to claims 17 and 20, above, apply equally to this claim.

Referring to claim 28, the remarks directed to claims 15 and 20, above, apply equally to this claim.

Referring to claim 29, the remarks directed to claims 18 and 20, above, apply equally to this claim.

Response to Arguments

6. Applicant's arguments filed January 29, 2003 have been fully considered but they are not persuasive. In light of the amendments to the claims, the examiner has included a new secondary reference, Chamberlin, which overcomes the applicant's new claims. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection. The arguments with respect to the remaining claims will be considered in spite of the new grounds.

Regarding the applicant's claim 15 arguments (page 15, 2d paragraph), Ozcelik's flexible approach evidences an improvement to Murphy in that Murphy fails to teach outputting the word address and bit address—the roadwork has been laid for this as shown by Ozcelik providing the details of addressing memory for storage and retrieval of data as done in Murphy.

Regarding the applicant's claim 3 arguments (page 16, 2d paragraph), Murphy discloses a clipping circuit that determines which coordinates fall outside a particular threshold. Digital logic devices generally communicate by means of digital signals. If there is no output from the circuit, it would serve no purpose.

Regarding the applicant's claim 4 arguments (page 16, 3d paragraph), where the inherent function of a device is to keep out signals that do not pass a certain threshold, it is unnecessary to explicitly mention the function.

Regarding the applicant's claim 7 arguments (page 17, 2d paragraph), the phrase "each register" (from col. 13, lines 15-16 of Murphy) means there is more than one register, and the phrase "has an associated address tag" means the more than one registers have more than one location in memory. The applicant also points out that "Nothing in Murphy appears to indicate

that any register or sub-portion thereof is mapped to two different addresses on the host bus" (page 18, 2d paragraph). As pointed out in the previous action, there are no addresses on the bus—it is merely a wire for transporting data.

Regarding the applicant's claim 8 arguments (page 18, 3d paragraph), the examiner is pointing out that Murphy does not use the ***term*** "address decoder." Regardless of the language used, if the functionality is the same, the applicant's invention is not novel as required by 35 U.S.C. 101. Moreover, the examiner is not using what the applicant is teaching against them as claimed in the first paragraph of page 19, but is only pointing out the scope of the applicant's claim. Also, regarding the applicant's claim on page 19, second paragraph that the Chiu address decoder does not monitor for writes, the examiner asserts that the "two-bit CONTROL signal" (from col. 3, lines 46-47 of Chiu) would have to be written there at some point, otherwise it would not exist.

Regarding the applicant's claim 14 arguments (page 20, 2d paragraph), the examiner has already dealt with this issue previously in this action.

Regarding the applicant's arguments on page 20, third paragraph, the applicant appears to be referring to claim 11, although they mention claim 14. The examiner has provided ample motivation to modify the teaching of Murphy, when it was pointed out that both references are directed to the generation and use of raster computer graphics, and therefore, Prouty simply provides details of the generation of a specific type of graphic, the type being more generally described and used by Murphy.

Regarding the applicant's claim 16 arguments (page 20, last paragraph), a multiplexer is a digital logic device that combines signals for transmission.

Regarding the applicant's claim 19 arguments (page 21, 2d paragraph), claim 18 references claim 17, which deals directly with this issue.

Regarding the applicant's arguments that the present action should be non-final in light of a lack of proper development, the examiner has provided a new grounds of rejection; moreover, the arguments were considered and were found non-persuasive.

The rejections to these claims stand.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Adam Arnold** whose telephone number is **703-305-8413**. The

examiner can normally be reached Monday-Thursday and alternate Fridays between 7:00 AM and 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Zimmerman, can be reached at (703) 305-9798.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

MARK ZIMMERMAN
SUPERVISORY PATENT EXAMINER
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